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Poly-GeSn Junctionless Thin-Film Transistors on Insulators Fabricated at Low Temperatures via Pulsed Laser Annealing

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High-performance polycrystalline GeSn (poly-GeSn) junctionless thin-film transistors (JL-TFTs) are proposed and fabricated at low process temperatures. Poly-GeSn thin films with a Sn fraction of 4.8% are prepared using cosputtering and pulsed laser annealing (PLA) techniques. The ultra-rapid nonequilibrium thermodynamic process with 25 ns PLA renders a good crystal GeSn thin film at a low temperature. The I_{ON}/I_{OFF} ratio increases by three orders of magnitude with GeSn channel thickness varying from 60 to 10 nm, suggesting that switch-off current is dominated by depletion width. A superior effective mobility of 54 $cm^2 V^{-1} s^{-1}$ is achieved for the JL-TFT with a 10 nm-thick GeSn film as a consequence of gate/channel interface passivation by oxygen plasma.

High-speed and low-power thin-film transistors (TFTs) for vertically monolithic 3D integrated circuits (3D-ICs) and flexible circuits are essential for next-generation electronics in the fields of displays, sensors, biodegradable electronics, and so on.[1–3] GeSn alloy has aroused significant attention due to its superior mobility and lower process temperature as compared with Si and Ge.[4–7] Polycrystalline GeSn (poly-GeSn), which could be fabricated on a large scale at a low cost, constitutes a suitable channel material of high-performance TFTs for next-generation displays, wearable devices, smart sensors, and so on.[8,9]

However, the most severe obstacle is to obtain high-quality poly-GeSn films on insulators with or without flexibility at a low process temperature. There are types of candidates for flexible substrates: ultrathin glass, metal foil, mica sheets, and plastic (polymer) films. Among these, due to better optical transmittance, flexibility, toughness, mass productivity, and lower cost, plastic substrates are ideal for flexible electronics or optoelectronics.[10] The plastic film candidates as flexible substrates include polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyimide (PI). Their glass transition temperatures are 110, 135, and 300 °C, respectively. To fabricate a poly-GeSn thin film at a low temperature (<300 °C) on insulators, techniques such as metal-induced crystallization (MIC),[11,12] pulsed laser annealing (PLA),[13,14] and solid-phase crystallization (SPC)[15–17] are widely adopted. Among these, the PLA technique is supposed to be a better method as it avoids metal contamination while keeping the substrates, especially flexible substrates, intact from heating damage. In the use of such a nonequilibrium technique that provides a local and super rapid annealing source, a high Sn fraction GeSn alloy with high crystallinity can be well fabricated,[18–20] even though for 1 at.% solid solubility of α-Sn in Ge.[21–23] Therefore, the PLA technique is a better choice to prepare high-quality poly-GeSn films at a low thermal budget.

To achieve sub-300 °C in the whole process of device fabrication, the design of a junctionless transistor, which was first put forward by Chi-Woo Lee et al. in 2009,[24] is introduced. In this structure, p/n junctions between the channel and source (S) or drain (D) are eliminated. Thus, high-temperature annealing for dopant activation in the S/D regions can be avoided. Therefore, this simple structure is found to be low-temperature process compatible and available for the continuing downscale to nanoscale in the future for TFTs.[25,26]

In this work, the preparation of poly-GeSn films at a low temperature and the fabrication and characterization of poly-GeSn junctionless TFTs (JL-TFTs) are carried out. Amorphous GeSn (a-GeSn) with different Sn chemical contents are deposited on Si substrates covered with 800 nm SiO_2 films by magnetron cosputtering and then annealed by pulse laser. The crystallinity and morphology of the GeSn films are characterized by Raman spectroscopy (spot size 4 μm, wavelength 532 nm), X-ray diffraction (XRD) patterns, scanning electron microscopy (SEM), and atomic force microscopy (AFM). Moreover, poly-GeSn JL-TFTs with a Sn fraction of 0.048 were fabricated and systematically analyzed. The maximum I_{ON}/I_{OFF} ratio with an ultralow I_{OFF} of 8×10^{-7} μA $μm^{-1}$ ($V_{DS} = -0.5$ V) was acquired at the cost of effective mobility degradation as the channel thickness

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reduced from 60 to 10 nm. A remarkable effective mobility of 54 $cm^2 V^{-1} s^{-1}$ in the 10 nm JL-TFT is achieved with the passivation of gate/channel interface assisted by oxygen plasma.

At the first step, a-$Ge_{1-x}Sn_x$ thin films are prepared on 800 nm SiO_2-covered silicon substrates. The deposition processes are carried out by direct current (DC) and radio frequency (RF) magnetron cosputtering with Sn and Ge targets, respectively. The substrates are cleaned three times in sequence with acetone and ethanol, and finally rinsed in deionized water four times. After drying, the substrates are immediately transferred into the magnetron sputtering chamber and ambient pressure is pumped to 10^{-4} Pa. The 300 nm-thick a-$Ge_{1-x}Sn_x$ films with Sn chemical content x of 0.02, 0.06, 0.15, and 0.2 are deposited at room temperature by maintaining a constant RF power of 100 W for the Ge target while adjusting the DC power from 1.3 to 16 W for the Sn target, respectively. At the second step, a-$Ge_{1-x}Sn_x$ is crystallized into poly-$Ge_{1-y}Sn_y$ by the PLA in nitrogen atmosphere using a 248 nm KrF excimer laser with an optimized energy density of 50 mJ cm^{-2}. It is found that a higher energy density would increase film roughness and even damage the film due to poor heat dissipation of the insulating substrate, whereas a lower energy density would not be enough for crystallization. To improve the crystallinity of GeSn films, multipulse PLA is introduced with the optimized ten pulses (see Figure S1, Supporting Information). The laser beam size is 4 × 25 mm and the pulse duration is 25 ns with a repetition rate of 1 Hz. To crystallize the a-GeSn films with the whole area, the holding stage is moved uniformly in two perpendicular directions with suitable step length.

Figure 1a shows the Raman spectra of GeSn films after a ten-pulse (10P) PLA process on a-$Ge_{1-x}Sn_x$ with Sn chemical content of 0.02, 0.06, 0.15, and 0.2, respectively. Obviously, all the GeSn films are crystallized with strong Ge–Ge mode peaks shown in the Raman spectra. However, the substitutional Sn fractions of poly-$Ge_{1-y}Sn_y$ films estimated from Raman spectra are consistently presented to be lower than the initial Sn chemical content of a-$Ge_{1-x}Sn_x$ due to the low solid solubility of α-Sn in Ge with Sn surface segregation, as shown in the inset. The black dashed line presents the initial Sn fraction in a-GeSn, and the red line with a scattered open rectangle presents the real Sn fraction in poly-GeSn. With the initial Sn chemical content increasing, the deviation of the final Sn fraction in poly-GeSn from the initial a-GeSn becomes larger. The data of the full-width at half maximum (FWHM) of the Ge–Ge mode peaks are also plotted in the inset. The FWHM of Ge–Ge Raman peak of poly-$Ge_{0.952}Sn_{0.048}$ from a-GeSn with an initial Sn content of 0.06 is narrowest, implying the highest crystallinity. In addition, the proper Sn fraction of 4.8% is supposed to improve the mobility without the consideration of severe alloy scattering as Sn fraction excess.[27–29] Therefore, high-crystallinity poly-$Ge_{0.952}Sn_{0.048}$ with an appropriate Sn fraction is suitable for the fabrication of high-speed TFT.

Moreover, as shown in Figure 1b, the XRD peaks of Ge (111) and (220) at 2θ of 27.64° and 45.82° are detected for the poly-Ge film treated by PLA with an energy density of 50 mJ cm^{-2} and 10P. The XRD peaks of GeSn (111) and (220) for poly-GeSn films shift to lower diffraction angles compared with the peaks from poly-Ge. The substitutional Sn fractions of poly-$Ge_{1-y}Sn_y$ films estimated from the XRD peaks of GeSn (111) and (220) are consistent with the data from Raman spectra. Additionally, the XRD peaks of GeSn (311) at 2θ at about 53° are difficult to be discerned due to the nearby background peaks.

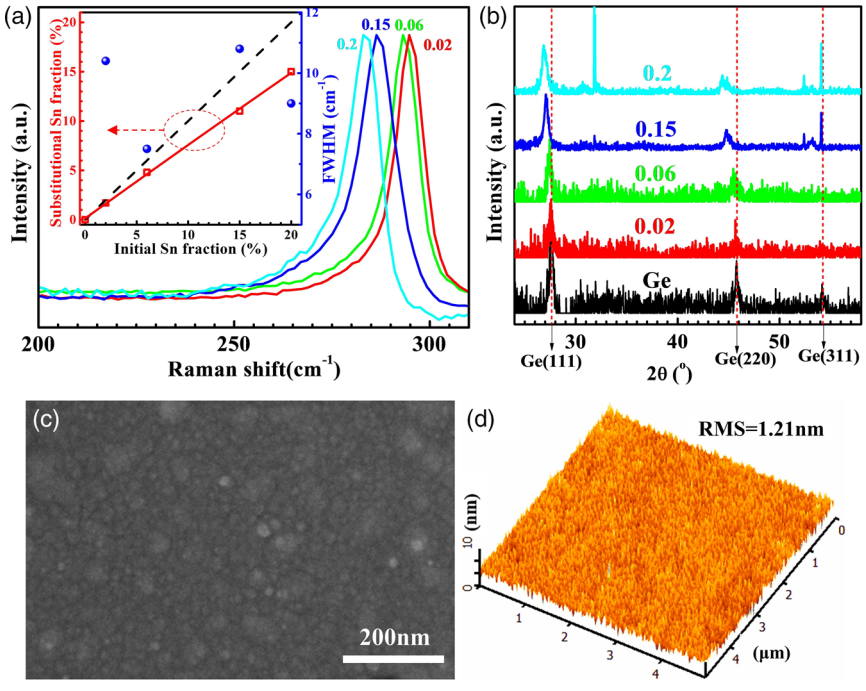

Figure 1. a) Raman spectra of poly-GeSn films fabricated from a-$Ge_{1-x}Sn_x$ (x = 0.02, 0.06, 0.15, 0.2) after PLA with an energy density of 50 mJ cm^{-2} and 10-pulse. The inset shows substitutional Sn fraction estimated from Raman spectra and XRD patterns also with FWHM of Ge-Ge peaks. b) XRD patterns of poly-GeSn films fabricated from a-$Ge_{1-x}Sn_x$ (x = 0.02, 0.06, 0.15, 0.2) after PLA with an energy density of 50 mJ cm^{-2} and 10-pulse. c) SEM and d) AFM images of 10-nm-thick poly-$Ge_{0.952}Sn_{0.048}$ films fabricated by PLA with an energy density of 50 mJ cm^{-2} and 10-pulse.

After etching off the surface-segregated Sn by 20% HCl aqueous solution for 2 min, poly-$Ge_{0.952}Sn_{0.048}$ films were visibly observed in SEM and AFM images as shown in Figure 1c,d. The film with a thickness of 10 nm is chosen as the representative, because all the films with various thicknesses exhibit slight differences in surface morphology and roughness. As the SEM image in Figure 1c suggests, the poly-GeSn film with 10P laser treatment exhibits a surface with bearable roughness. With a more precise characterization by the AFM image as shown in Figure 1d, the root-mean-square (RMS) of surface roughness is measured to be 1.21 nm, only 0.19 nm rougher than that of the as-annealed (see Figure S2, Supporting Information), and meets the requirement for the fabrication of TFTs.

An ultrathin channel material is required for the device to turn off and attain low static power consumption. The maximum depletion layer width W_m can be approximated as

$$W_m = \sqrt{\frac{4\varepsilon_s kT \ln(N_B/n_i)}{q^2 N_B}} \quad (1)$$

where $\varepsilon_s, k, T, N_B, n_i, q$ are the permittivity of the semiconductor, Boltzmann constant, temperature, impurity concentration, intrinsic carrier concentration of the semiconductor, and elementary charge, respectively. The intrinsic carrier concentration of $Ge_{0.952}Sn_{0.048}$ is about $5.3 \times 10^{13}\ cm^{-3}$ calculated in previous studies.[30]

$$n_i = (N_C N_V)^{1/2} \exp\left(-\frac{E_g}{2kT}\right) \quad (2)$$

where N_C and N_V are the effective density of states for the conduction band and valence band, respectively. Since the Sn fraction is very low, the N_C and N_V of $Ge_{0.952}Sn_{0.048}$ are regarded as 1.04×10^{19} and $6.0 \times 10^{18}\ cm^{-3}$, the same as that of Ge.[31] E_g is the bandgap of $Ge_{0.952}Sn_{0.048}$, which is estimated to be 0.618 eV. The unintentionally doped carrier in poly-GeSn is identified as a hole due to the intrinsic defects existing in the poly-GeSn film during formation. In this case, hole concentration in poly-$Ge_{0.952}Sn_{0.048}$ is larger than $10^{18}\ cm^{-3}$ and less than $10^{19}\ cm^{-3}$, as measured by Hall effect measurement. Therefore, W_m of poly-$Ge_{0.952}Sn_{0.048}$ is estimated to be 11–29 nm. To study the effect of channel thickness on characteristics of devices, four devices with poly-GeSn channel thicknesses (T) of 10, 15, 20, and 60 nm are fabricated for comparison. Even the GeSn film is as thin as 10 nm; the temperature at the GeSn/substrate interface never reaches over the 300 °C limit as demonstrated by the simulation (see Figure S3, Supporting Information).

Figure 2a shows the key fabrication steps of p-type poly-GeSn JL-TFTs. First, the GeSn materials for channel and S/D regions in the TFTs were patterned by laser microwriter with sputtering and lift-off processes. The channel width and length are 20 and 12 μm, respectively. The initial Sn chemical content in a-GeSn is chosen to be 0.06 as the optimal proportion. Then the PLA treatments with the energy density of $50\ mJ\ cm^{-2}$ and 10P were carried out to form poly-$Ge_{0.952}Sn_{0.048}$ films. After cleaning in a dilute HCl solution, Cr/Au (5/100 nm) electrodes with Au on the top are deposited on the S/D regions by sputtering. Thanks to the large contact area of S or D ($>200 \times 200$ μm) and the p-type GeSn films, Ohmic contact is successfully obtained. Then, a 5/15 nm Al_2O_3/HfO_2 gate stack with HfO_2 on the top is deposited using atomic layer deposition (ALD) at 150 °C. A 50/50 nm Au/TaN gate contact with Au on the top is formed by sputtering. For the gate/channel interface passivation samples, in situ remote O_2 plasma is introduced to pretreat poly-$Ge_{0.952}Sn_{0.048}$ surface prior to gate stack deposition in the ALD chamber. The plasma source apparatus is Litmas Remote Plasma Source from Advanced Energy, integrating a cylindrical inductive plasma source and a solid-state RF power delivery system. RF power, O_2 flow rate, pressure, and substrate temperature are set as 2500 W, 120 sccm, 7 hPa, and 150 °C, respectively. O_2 plasma is carried by Ar. Finally, the top oxide layers on S/D regions are removed by etching for measurements. Compared with the classical metal-oxide-semiconductor field effect transistor (MOSFET) fabrication, the JL transistor process is simpler without doping for the formation of a p/n junction as schematically shown in Figure 2b. Figure 2c shows a photographic top view of fabricated poly-GeSn TFTs with a channel width and length of 20 and 12 μm, respectively.

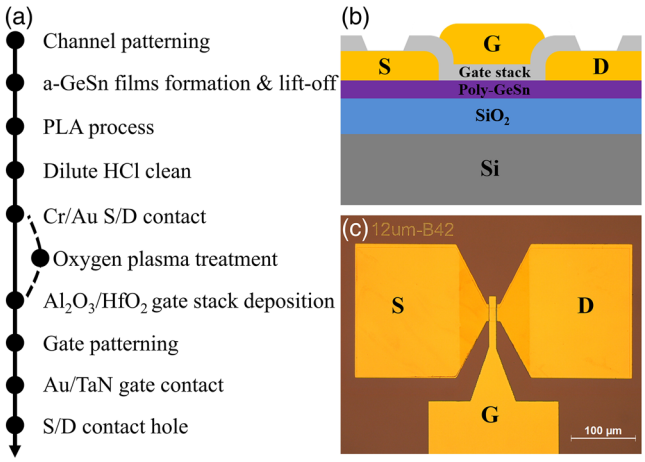

Figure 2. a) Process flow, b) cross-sectional view of the device structure and c) photographic top view of the fabricated p-type poly-GeSn TFT.

Figure 3 shows the typical transfer curves and output curves for devices with a GeSn channel thickness of 60, 20, 15, and 10 nm, respectively. In the characterization of transfer curves, the drain is biased at −0.5 V. The transfer curve of TFT with a channel thickness of 60 nm is plotted in Figure 3a. The channel thickness is much larger than the maximum depletion layer width, sot the device cannot be shut off effectively, and the I_{ON}/I_{OFF} ratio is very low with the off-state current density greater than $0.5\ \mu A\ \mu m^{-1}$. Figure 3b shows the output characteristic of TFT with a channel thickness of 60 nm. Although the gate voltage has certain regulation function, the device does not reach saturation with poor performance. The I_{ON}/I_{OFF} ratio of TFTs with a channel thickness of 20 nm has improved, but still less than an order of magnitude, as shown in Figure 3c. It suggests that the thickness of 20 nm is still greater than the maximum depletion layer width, and the doping concentration of poly-GeSn should be greater than $10^{18}\ cm^{-3}$. Figure 3d shows that the output characteristic is also improved. As the channel thickness reduces to 15 nm, the I_{ON}/I_{OFF} ratio of TFT is about 1.5×10^2 with I_{OFF} of $3.2 \times 10^{-5}\ \mu A\ \mu m^{-1}$, as shown in Figure 3e. The output characteristic, as shown in Figure 3f,

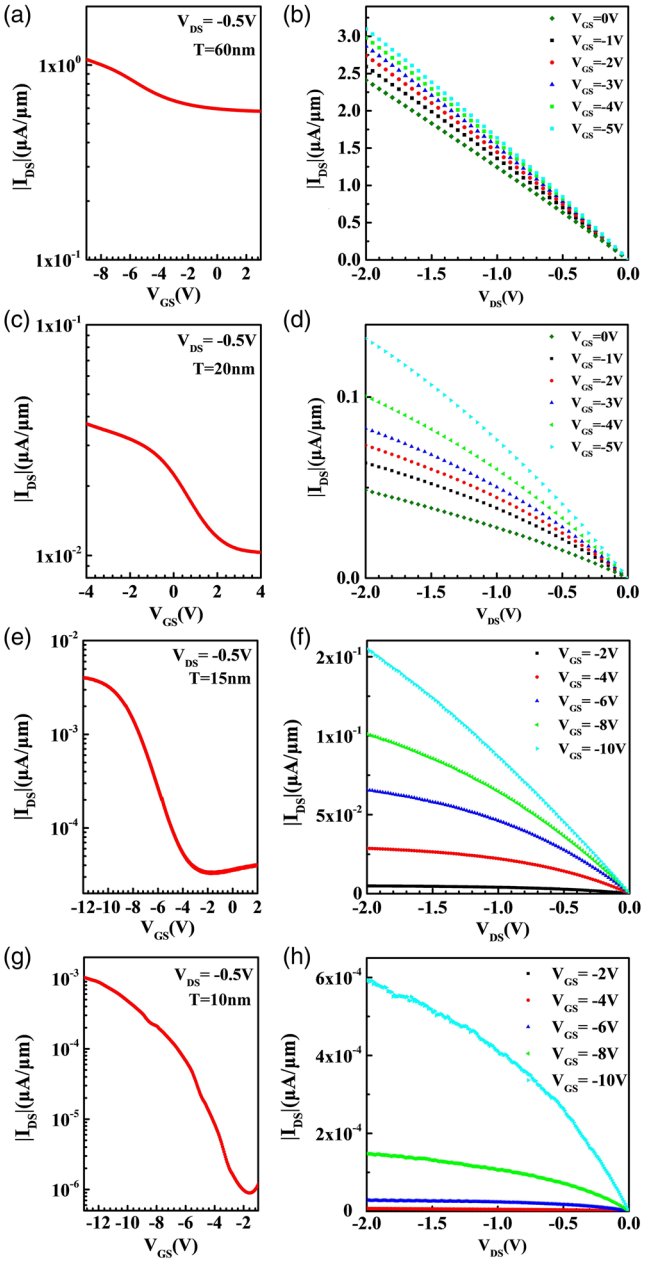

Figure 3. a,b) Transfer curves and output curves for the device with a GeSn channel thickness of 60 nm. c,d) Transfer curves and output curves for the device with a GeSn channel thickness of 20 nm. e,f) Transfer curves and output curves for the device with a GeSn channel thickness of 15 nm. g,h) Transfer curves and output curves for the device with a GeSn channel thickness of 10 nm.

exhibits a typical transistor performance. Nevertheless, I_{ON} also declines slightly as the film thickness decreases to 15 nm. This is ascribed to the reduced quantity of in-film carriers and serious mobility reduction caused by interface scattering as the film thickness decreases. For TFTs with a 10 nm-thick poly-GeSn channel, as shown in Figure 3g,h, the I_{ON}/I_{OFF} ratio is further improved to be 1.5×10^3 with I_{OFF} as low as 8×10^{-7} μA μm^{-1}, which is lower than that of a 15 nm-thick channel TFT by one order of magnitude. Therefore, the poly-GeSn film is supposed to be fully depleted at the off state and the actual W_m is estimated to be between 10 and 15 nm. According to the transfer characteristic curves, the threshold voltage decreases gradually as the channel thickness varies from 60 to 10 nm, suggesting the enhancement of device performance as I_{OFF} decreases in a larger degree than I_{ON}. Moreover, the threshold voltage even reaches a negative regime. This is because the threshold voltage is not only determined by the doping type in the channel but also strongly affected by the gate electrode work function. In this work, the gate electrode is TaN/Au with TaN contacting the gate oxide stack. As suggested by the literature,[32] the work function of TaN varies in a large range from 3.4 to 4.7 eV depending on the nitrogen content in TaN and the formation process. Therefore, the work function of TaN we deposit might be near the mid-bandgap of GeSn, resulting from the predepletion of the p-channel and even a negative turn-off voltage.

Figure 4 shows the sub-threshold voltage swing (SS), Hall mobility (μ_{Hall}), effective mobility (μ_{eff}), and I_{ON}/I_{OFF} ratio dependence of GeSn thickness. As shown in Figure 4a, SS decreases monotonously as the film thickness reduces from 60 to 10 nm, indicating that controllability of the gate is enhanced as the film thickness decreases. The effective mobility of TFTs was extracted by

$$\mu_{eff} = \frac{L}{WC_{ox}(V_{GS} - V_T)} \times \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=\text{constant}} \quad (3)$$

where W and L are the channel width and length, respectively, C_{ox} is gate oxide capacitance, and V_T denotes threshold voltage. As shown in Figure 4b, μ_{Hall} reaches 205 cm^2 V^{-1} s^{-1}, indicating a high crystal quality of poly-GeSn films. Furthermore, μ_{Hall} and μ_{eff} decrease sharply with a decrease in GeSn film thickness (T), and μ_{eff} is always lower than μ_{Hall}. μ_{eff} remains around 90 cm^2 V^{-1} s^{-1} when the channel thickness of the device is greater than 20 nm, and μ_{eff} decreases sharply to 24.3 and 0.03 cm^2 V^{-1} s^{-1} for the devices with channel thicknesses of 15 and 10 nm, respectively. This can be ascribed to a serious interface scattering as film thickness decreases. Thus, interface passivation is necessary for the improvement of device performance with high effective carrier mobility.

The oxygen plasma is used to passivate the interface for the TFT with a poly-GeSn channel thickness of 10 nm. The plasma treatment conditions are described in detail in the experimental part earlier. The surface of poly-GeSn was pretreated for 90 s using in situ oxygen plasma before the stacked gate dielectric layers were deposited with ALD. **Figure 5** shows the transfer and output characteristics of the passivated GeSn TFT. The I_{ON}/I_{OFF} ratio of the device with oxygen plasma treatment is about 10^2, and the effective carrier mobility, μ_{eff}, is extracted to be about 54 cm^2 V^{-1} s^{-1}, which is improved by 1800 times compared with the device without interface passivation. As is well known, current can be expressed as follows

$$I = Nq\mu E \quad (4)$$

where N, q, μ, and E present the number of carriers, elementary charge, mobility, and electric field, respectively. Since μ increases by three orders of magnitude after interface passivation whereas

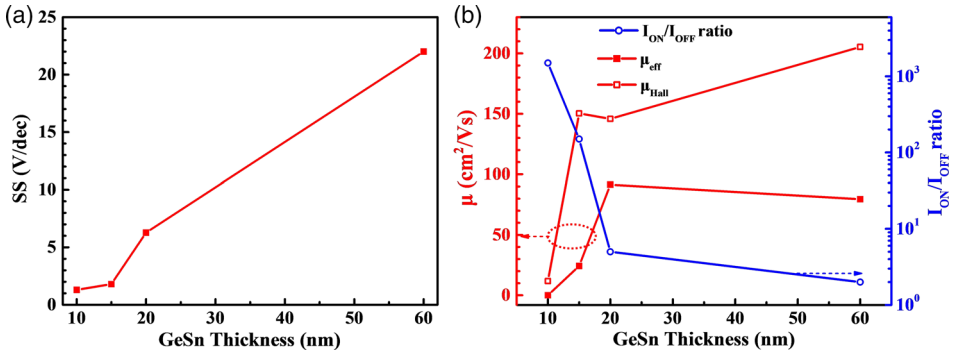

Figure 4. a) SS, b) Hall mobility, effective mobility, and I_{ON}/I_{OFF} ratio dependence on GeSn thickness.

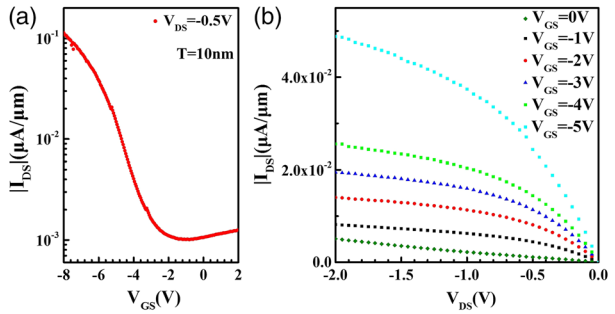

Figure 5. Transfer curves and output curves for a 10-nm-thick poly-GeSn channel TFT with surface treated by oxygen plasma before deposition of gate dielectric layers.

the other parameters remain the same, the total current should be increased by three orders of magnitude as well. Therefore, I_{OFF} is enlarged by 1.1×10^3 magnitude after interface passivation. However, I_{ON} is enhanced by 1×10^2 magnitude. This can be ascribed to channel thickness thinning by partial oxidization of the poly-GeSn channel during oxygen plasma pretreatment and the slight variation of crystallinity and carrier concentration among the samples caused by energy fluctuation of the pulsed laser.

We compare the device characteristics in terms of mobility, I_{ON}/I_{OFF} ratio, process temperature, and Sn fraction of poly-GeSn with other similar works in **Table 1**. Although there is room for improvement of the I_{ON}/I_{OFF} ratio compared with the other works, the process temperature in this work is the lowest and below 300 °C, whereas that of all the others is 500 °C, which is much higher than the highest withstand temperature of plastic flexible substrates. Furthermore, the peak mobility in our work is 54 $cm^2 V^{-1} s^{-1}$, which is the second record highest mobility of poly-GeSn TFTs so far and the record highest mobility of poly-GeSn TFTs as regards the sub-300 °C process temperature to date. Therefore, the devices in this work are promising candidates for the final realization of flexible devices.

Table 1. Comparison of poly-GeSn TFT characteristics in this work to the reported references to date.

	Peak mobility [$cm^2 V^{-1} s^{-1}$]	I_{ON}/I_{OFF} ratio	Process temperature [°C]	Sn fraction of poly-GeSn [%]
Ref. [33]	162.2	2.8×105	500	5.1
Ref. [34]	39.3	1.7×10^4	500	5
Ref. [35]	25	10^3	500	3
Ref. [36]	19	2×10^3	500	0
This work	54	1.2×10^2	Sub-300	4.8

In summary, we have prepared poly-$Ge_{0.952}Sn_{0.048}$ films with high crystallinity using cosputtering and multipulse PLA techniques at a low process temperature. The p-type poly-GeSn JL-TFT is proposed to be a simple and low-cost method with a low thermal budget. As the thickness of poly-GeSn decreases, the I_{ON}/I_{OFF} ratio increases, whereas the effective mobility is reduced. After the passivation of the gate/channel interface by oxygen plasma, the mobility of JL-TFT with a 10 nm-thick channel is improved up to 54 $cm^2 V^{-1} s^{-1}$, exhibiting an outstanding performance as TFTs. The whole process of material and device preparation is available to 3D-IC and flexible circuits.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

GeSn, junctionless thin-film transistors, pulsed laser annealing

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